Design calculations for robust I2C communications

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For many systems that require reliable non-volatile storage, EEPROM is the memory technology of choice. EEPROM features a robust architecture, with multiple suppliers and many years of refinement. EEPROM devices are available in a variety of industry-standard serial buses, including I^2C, SPI, Microwire, and the UNI/O bus. Due to its widespread hardware support in microcontrollers and other chipsets, and the fact that its easy signaling enables efficient implementation with minimal silicon, the I^2C bus comprises approximately 70% of the non-volatile memory market. The I^2C bus topology relies on correctly sized pull-up resistors for reliable, robust communications, however. Selecting the wrong resistor values can not only result in wasted power, but can also lead to erroneous bus conditions and transmission errors caused by noise or changes in temperature, operating voltages, and by manufacturing variations between devices.

I^2C is a two-wire synchronous bus with the serial clock line (SCL) line used as a clock, produced by the bus master. The serial data line (SDA) is used for bi-directional data transfer. The data line is modified while the clock is in specific states, to indicate the start and stop of transmissions and avoid additional lines. The I^2C bus is built around open-collector outputs, where a device can pull a line low through a transistor to ground (see figure 1). This allows easy arbitration over control of the bus, enabling the implementation of bi-directional communications on a single data line and multi-master support. As shown in Figure 1, each line has an external resistor to the supply voltage V_{dd} that pulls the line high when released or idle.

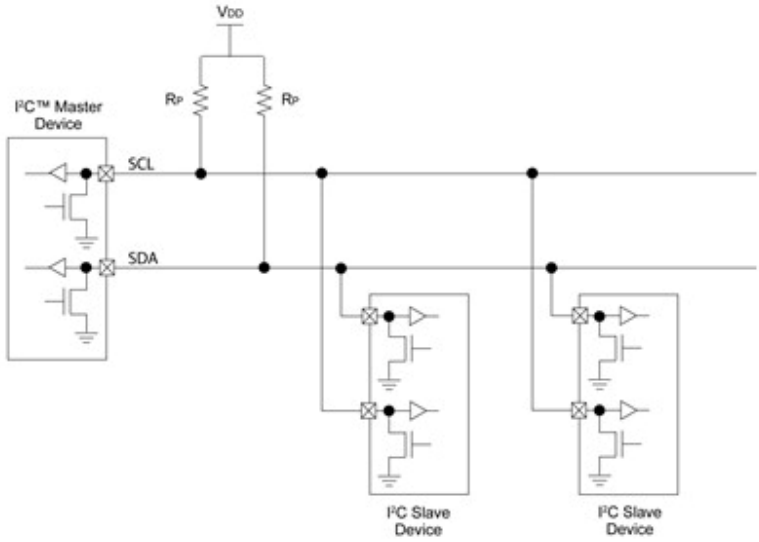

Figure 1: I^{2}C bus topology

The three factors to consider when determining the pull-up resistor values (R_p) are:

- Supply voltage (V_{dd})
- Total bus capacitance (C_{BUS})
- Total high-level input current (I_{IH})

Let's calculate the ideal pull-up resistor values for the following example conditions:

- Supply voltage (V_{dd}) of 5 V
- Clock frequency of 400 kHz
- Bus capacitance of 100 pF

Supply voltage (V_{dd})

First, let's take a closer look at the effect of the supply voltage V_{dd}. The I^{2}C specification defines a voltage below V_{IL}, or 30% of the supply voltage, as a logical low and, likewise, above V_{IH}, or 70% of the supply voltage, as a logical high (see figure 2). A voltage between these two levels leads to an undefined logic level. In reality, the pin will read either logical high or low in this range, but it may vary among devices with temperatures, voltages, noise sources, and other environmental factors influencing the logic levels.

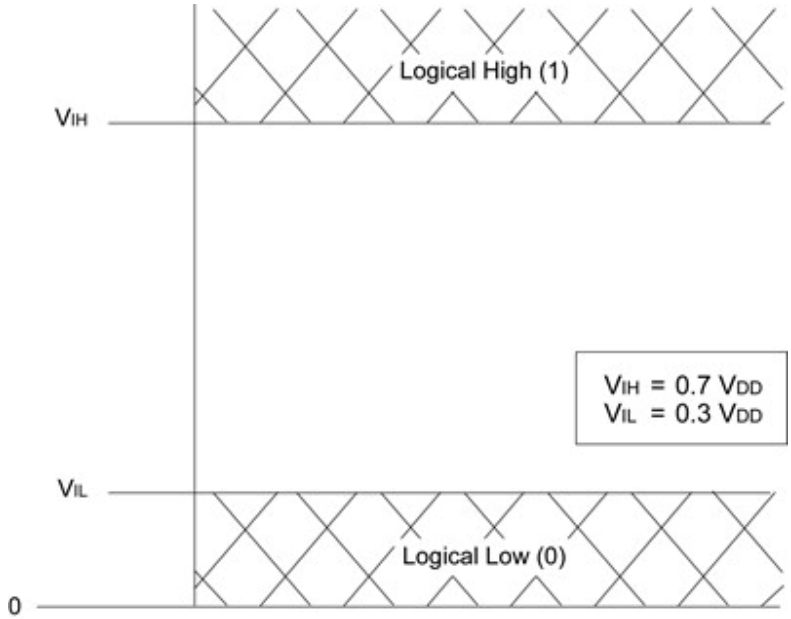

Figure 2: Specified voltage levels for logical high and low

The supply voltage limits the minimum R_p value for which the bus can be pulled low. A strong pull-up will prevent a device from being able to bring the line sufficiently low, to ensure a logical low is detected. This is caused by the potential divider formed between the pull-up resistor and the on-resistance of the transistor to ground (see figure 3). The on resistance of the transistor is not typically specified. Instead, a maximum sink current (I_{OL}) is given for which the voltage drop across the transistor is below the output logical low-voltage level (V_{OL}).

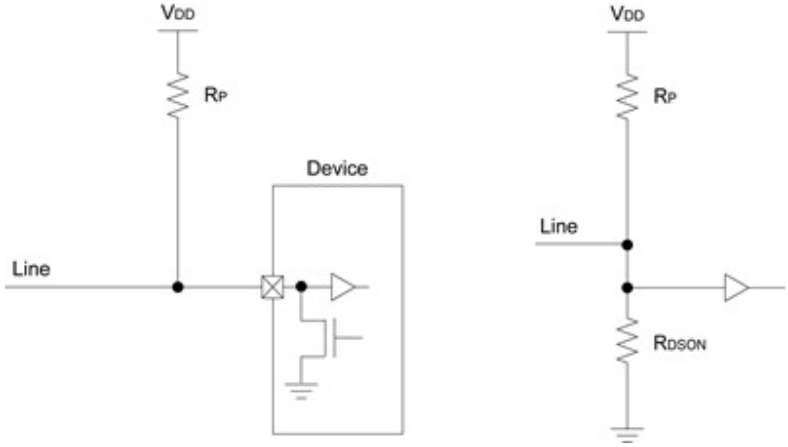

Figure 3: Open-collector topology and equivalent circuit

If we apply Ohm's law we obtain the minimum pull-up resistance, allowing the bus to be pulled low:

$$Rp \geq \frac{Vdd - V_{OL}}{I_{ol}} \qquad [1]$$

$$\geq 1.533\ K\Omega$$

For commercially-available I^2C EEPROM devices, the typical V_{OL} specification is a maximum of 0.4 V at an I_{OL} of 3 mA. For the case in which multiple devices are connected on the same bus, the minimum R_p is determined by the device with the lowest sink current.

Total Bus Capacitance (Cbus)

On the SCL and SDA lines, the capacitance includes all pins, connections, PCB traces, and wire. We refer to this combination as the bus capacitance, and for long traces and cabling, this can be significant. The open-collector topology requires the external resistor to pull the line high when released. The pull-up resistor, coupled with the bus capacitance, has an RC time constant that limits the rise time. This effect grows with increasing clock frequency, because less time is available for the line to rise. If the selected resistor value is too high, the line may not rise to a logical high before it is next pulled low. This is an important consideration for designs that feature many devices on a single bus, which often have higher bus capacitance.

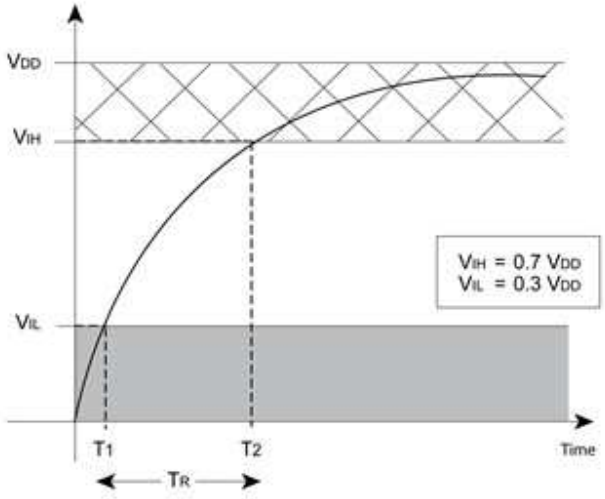

Figure 4: Charge time for transition between logical low to high

We can calculate bus capacitance from PCB trace lengths and published pin capacitance, or measure it using capacitance probes or smart tweezers. If a precise calculation or measurement of the bus capacitance is not possible, an overestimated worst-case reading should provide a safe maximum-resistance value.

Equation 2 is the general equation used to determine the voltage *V* across a charging capacitive load as a function of time. This allows for the calculation of the time required

for the bus voltage to rise to a particular value, for a specific pull-up resistance and bus capacitance.

$$V(t) = Vdd\left(1 - e^{-t/RC}\right) \qquad [2]$$

Solving for time, we obtain

$$t = -RC\ln\left(1 - \frac{V(t)}{Vdd}\right) \qquad [3]$$

We can then calculate the time (T_1) for the voltage to rise to V_{IL}; the time (T_2) to rise to V_{IH}; and, critically, the charge time for transition between these two levels (T_R, see figure 4). Since both V_{IL} and V_{IH} are products of Vdd, the equation is independent of supply voltage, since the Vdd terms cancel out.

Solving for V_{IL}, we obtain

$$V_{IL} = 0.3 \times Vdd \Rightarrow T_1 = 0.356675 \times RC \qquad [4]$$

Solving for V_{IH}, we obtain

$$V_{IH} = 0.7 \times Vdd \Rightarrow T_2 = 1.203970 \times RC \qquad [5]$$

We then calculate T_R as

$$T_R = T_2 - T_1 = 0.847298 \times RC \qquad [6]$$

The maximum rise time for a variety of operating voltages is specified by the I^2C standard, and is determined by the pull-up resistance. From this time and the bus capacitance, we can calculate the maximum allowable pull-up resistance (R_p). For a 400 kHz clock frequency at 5 V, the specified maximum rise time, (T_R), is 300 ns, given the bus capacitance C_{BUS} of 100 pF.

$$\begin{aligned} R_P &\le \frac{T_R}{0.847298 \times C_{BUS}} \\ &\le \frac{300 \times 10^{-9}}{0.847298 \times 100 \times 10^{-12}} \\ &\le 3.541K\Omega \end{aligned} \qquad [7]$$

Total high-level input current (I_{IH})

Even when no device is pulling down the line and it is a logical high, current continues to flow through the pull-up resistors. This current is caused by the leakage of the digital inputs of the devices on the bus, from low quality PCB materials, and possibly from soldering residues. Some of these cannot be foreseen, but, assuming quality materials and

good manufacturing practices, the input pin leakage is dominant.

From Figure 2, the line needs to be above V_{IH} to be regarded as logical high, when there are no devices pulling the bus low. The leakage current limits the maximum value of R_p, such that the voltage drop across it does not prevent the line from being pulled above V_{IH}. It is also prudent to allow some guard margin on the V_{IH} specification, to prevent noise spikes from bringing the voltage below the V_{IH} level. For robust operation in a high-noise environment, the I^2C specification recommends 0.2 *V*dd as a suitable margin above V_{IH}.

Additional margin over logical high input level.

$$\begin{aligned} V_{HMAR} &= 0.2 \times Vdd \\ &= 0.2 \times 5V \\ &= 1V \end{aligned} \qquad [8]$$

The leakage of digital inputs is normally given in the datasheet of devices and, for Microchip's I^2C EEPROM devices, the maximum input leakage current (I_{LIEE}) is 1 µA. The minimum components for a system are a microcontroller I^2C master and an I^2C slave device. For this example, assuming a microcontroller with 1 µA input leakage (I_{LIMCU}) and four I^2C EEPROM devices, and allowing 100% margin, I_{IH} is 10 µA.

We can define the leakage current due to pin leakages for defined bus as:

$$\begin{aligned} I_{IH} &= (1 + M\,\text{arg}\,in) \times (I_{LIMCU} + (4 \times I_{LIEE})) \\ &= (1+1) \times (1 + (4 \times 1))\mu A \\ &= 10\mu A \end{aligned} \qquad [9]$$

Applying Ohm's law, we can determine the maximum value for R_p that will meet these specifications

$$\begin{aligned} R_P &\le \frac{Vdd - (V_{IH} + V_{HMAR})}{I_{IH}} \\ &\le \frac{5.0 - (3.5 + 1.0)}{10 \times 10^{-6}} \\ &\le 50K\Omega \end{aligned} \qquad [10]$$

Resistor value calculation

From the supply voltage (equation 1), the bus capacitance (equation 7) and the leakage calculations (equation 10), we have a range of values for R_p:

$$1.533\ \text{k}\Omega \le R_p$$
$$R_p \le 3.541\ \text{k}\Omega$$
$$R_p \le 50\ \text{k}\Omega$$

How do we decide which to use? The 50 kΩ maximum caused by the leakage current

can be discarded, since the bus capacitance dominates. As a result, the range of acceptable resistor values is:

$$1.533\ \text{k}\Omega \leq R_p \leq 3.541\ \text{k}\Omega$$

Designers should choose a value near the middle of the range, to provide as much guard banding as possible. For this example, a 2.2 kΩ pull-up resistor would be ideal.

The pull-up resistors must be reduced in size when increasing the bus speed or when there is significant bus capacitance. The lower-value resistors cause increased current draw, as each logical low on the bus creates a path to ground, negatively impacting power consumption. The bus speed can become a trade-off between completing tasks quickly and returning a system to a low-power idle state versus the additional current draw created by the higher bus speed requirements. For applications with very low power budgets, SPI may be a better-suited bus protocol, since it uses driven lines, instead of open collectors. For many applications, however, I^2C with the correct choice of pull-up resistor delivers an efficient, accurate, compact solution.

About the authors

Chris Parris and Jonathan Dillon are senior applications engineers at Microchip Technology Inc.